1.1. Digital Down Conversion (DDC)

The Analog-to-Digital Converter (ADC) block sub-samples Intermediate Frequency (IF) signals and a Digital Down Conversion (DDC) block converts the IF to base-band signal.

In normal cases, the tuner is high side mixing and the spectrum is inverted. The demodulator requires an inverse spectrum in the DDC (register spec_inv). In RTL2832U there is an adjacent channel canceller that is enabled or disabled by register en_aci. The initial IF frequency should be set by register pset_iffreq. This register setting depends on the crystal frequency. The equation of pset_iffreq is shown below:

\[ pset\_iffreq = -floor\left(\frac{f_{IF,D}}{f_{crystal}} \times 4194304\right) \]

where:

- \( f_{IF,D} \): Intermediate Frequency (IF) after sub-sampling
- \( f_{crystal} \): Crystal frequency

Examples:

- \( f_{IF}=4.57M, f_{ADC}=28.8M, pset\_iffreq= -665554 =2^{22} - 665554 = 3528750 \) (two’s complement) = 0x35D82E
- \( f_{IF}=36.167M, f_{ADC}=28.8M, f_{IF,D}=36.167-28.8= 7.367, pset\_iffreq= -1072897 =2^{22} - 1072897 =3121407 \) (two’s complement) = 0x2FA0FF
- \( f_{IF}=36.125M, f_{ADC}=28.8M, f_{IF,D}=36.167-28.8= 7.367, pset\_iffreq= -1066780 =2^{22} -1066780 =3127524 \) (two’s complement) = 0x2FB8E4
- \( f_{IF}=0M, f_{ADC}=28.8M, \)
\( pset\_iffreq = 0x0 \)

- **DAB mode:**
  \( pset\_iffreq = -1066988 = 3127316 \) (two’s complement) = \( 0x2FB814 \)

### Table 1. Digital Down Conversion (DDC)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Page</th>
<th>Offset{MSB,LSB}</th>
<th>Bits Used</th>
<th>R/W</th>
<th>Default (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>spec_inv</td>
<td>1</td>
<td>0x15</td>
<td>[0]</td>
<td>R/W</td>
<td>0</td>
<td>1: Spectrum inversion 0: Spectrum non-inversion</td>
</tr>
<tr>
<td>en_aci</td>
<td>1</td>
<td>0x15</td>
<td>[1]</td>
<td>R/W</td>
<td>1</td>
<td>1: Enable adjacent channel rejection 0: Disable adjacent channel rejection</td>
</tr>
<tr>
<td>pset_iffreq</td>
<td>1</td>
<td>{0x19,0x1B}</td>
<td>[21:0]</td>
<td>R/W</td>
<td></td>
<td>Set IF frequency</td>
</tr>
</tbody>
</table>

### 1.2. Resampler

As the ADC sampling clock is larger than the symbol ratio, there is a re-sampler to convert data of sampling rate to symbol ratio. The ratio could be set by register “rsamp\_ratio”. The \( rsamp\_ratio \) is related with signal bandwidth and crystal frequency. The equation of \( rsamp\_ratio \) is shown as below,

\[
rsamp\_ratio = \text{floor} \left( \frac{f_{\text{crystal}}}{f_{\text{symbol}}} \times 4194304 \right)
\]

where \( f_{\text{crystal}} \) = crystal frequency
\( f_{\text{symbol}} \) = symbol ratio of different bandwidths

- **BW: 8MHz** \( f_{\text{symbol}} = \frac{64}{7} \text{ MHz}, f_{\text{crystal}} = 28.8\text{MHz} \)
  - \( rsamp\_ratio = 13212057 \) (dec) = \( 0xC99999 \)

- **BW: 7MHz** \( f_{\text{symbol}} = 8 \text{ MHz}, f_{\text{crystal}} = 28.8\text{MHz} \)
  - \( rsamp\_ratio = 15099494 \) (dec) = \( 0xE66666 \)

- **BW: 6MHz** \( f_{\text{symbol}} = \frac{48}{7} \text{ MHz}, f_{\text{crystal}} = 28.8\text{MHz} \)
  - \( rsamp\_ratio = 17616076 \) (dec) = \( 0x10CCCC \)

- **DAB mode:**
  - \( rsamp\_ratio = 14745600 \) (dec) = \( 0xE10000 \)

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Page</th>
<th>Offset{MSB,LSB}</th>
<th>Bits Used</th>
<th>R/W</th>
<th>Default (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rsamp_ratio</td>
<td>1</td>
<td>{0x9F, 0xA2}</td>
<td>[27:2]</td>
<td>R/W</td>
<td>C99999</td>
<td>resampler ratio</td>
</tr>
</tbody>
</table>