

Why your high-speed ADC can never have enough SNR

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One of the most important parameters in a radio is the noise floor, or the receiver's noise figure. These parameters determine the lowest signal strength of very weak input signals that the receiver can still recover successfully. If the receiver noise within the demodulated bandwidth is larger than the received signal itself, the weak input signal cannot be demodulated. In order to "elevate" the weak signal of interest above the receiver noise floor (**Figure 1**), either the transmit signal power must be increased or the noise floor of the receiver must be reduced. In many applications, such as a radar system or cell phone, the transmitter and receiver are completely isolated from each other. Thus, the only option to further improve the receiver sensitivity is to improve the noise figure.

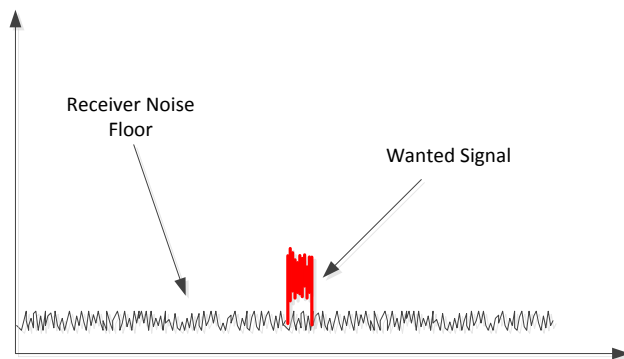


Figure 1: Weak wanted signal in sensitivity scenario.

Better receiver sensitivity leads to better target detection and identification in radar systems, or an increased ability for electronic intelligence (ELINT) receivers to recover enemy communications in the presence of strong jammers. In the wireless communications sector, better sensitivity enables wider coverage range for base stations. Better sensitivity also increases cell phone battery life, as excess transmit power is preserved.

Improve receiver noise figure

A high-speed analog-to-digital converter (ADC) typically has the largest noise figure of all components in the receiver signal chain. Its contribution to the system noise figure can be reduced greatly by adding more gain (with a low noise figure) upfront using low-noise amplifiers (LNAs). However, this method cannot be used in a blocking scenario. In the presence of a large in-band interferer or jammer that can't be filtered out, the gain in the signal chain must be reduced in order to avoid saturation of the ADC input. Therefore, the only way to really improve the receiver noise figure is to improve the noise floor by using a data converter with a better signal-to-noise ratio (SNR), as shown in the example in **Figure 2**.

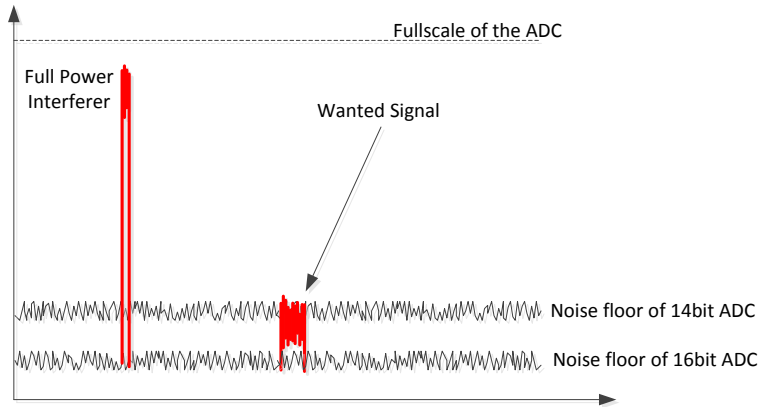


Figure 2: Advantage of lower noise floor with a 16-bit ADC for a weak desired signal in the presence of a strong blocker.

The ADC's noise figure is basically the difference of the ADC noise spectral density (NSD), or noise floor, in decibel milliwatts/Hertz (dBm/Hz) to the absolute thermal noise density (kT in dBm/Hz) normalized to a 1-Hz bandwidth. It can be calculated using Equation 1:

$$\begin{aligned}
 NF_{ADC} &= P_{FULLSCAE} [dBm] - NSD_{ADC} [dBFS / Hz] - kTB [dBm] = \\
 &P_{FULLSCAE} [dBm] - SNR_{ADC} - 10 \cdot \log\left(\frac{FS}{2}\right) + 174 dBm \\
 P_{FULLSCAE} [dBm] &= 10 \cdot \log\left(1000 \cdot \frac{(V_{pp})^2}{8 \cdot Z_{IN}}\right) \quad (1)
 \end{aligned}$$

where k = Boltzmann's constant, T = temperature in Kelvin, and T = 290 K for room temperature.

Using these formulas, one can calculate the equivalent noise figure for two modern-day ADCs (**Table 1**): a 16-bit, 250-MSPS (ADS42JB69) and a 16-bit, 1-GSPS (ADS54J60).

Full-scale SNR refers to the SNR at low frequencies in the presence of a full-scale input signal (for example, an interferer). The noise floor is often displayed as NSD. The noise of the entire Nyquist zone is normalized to a bandwidth of 1 Hz.

Parameter	ADS42JB69	ADS54J60
Sampling rate (FS)	250 MSPS	1 GSPS
Resolution	16 bit	16 bit
Input full scale (Vpp)	2 Vpp	1.9 Vpp
Full-scale SNR	74.0 dBFS	71.1 dBFS
Input impedance (Z _{IN})	200 Ω	200 Ω
Calculated noise figure	23.0 dB	19.5 dB
NSD	-155 dBFS/Hz	-158.1 dBFS/Hz

Table 1: Noise figure and noise floor comparison between 16-bit 250 Msps and 16-bit 1 Gsps ADCs

For comparison, the SNR of the ADS42JB69 is almost 3 dB better; however, the Nyquist zone of the ADS54J60 is three times larger. As a result, its NSD is 3.1 dB better and is approaching -160 dBFS/Hz, which is a very good value for a high-speed pipeline ADC. Together with the slightly smaller input full-scale signal swing, the noise figure of the ADS54J60 is 3.5 dB better than the ADS42JB69.

What determines ADC thermal noise?

The ADC's noise floor is determined by three different noise contributors: quantization, thermal noise and clock jitter.

The quantization noise impact (which originates from the rounding error of the least significant bit [LSB]) is usually very small, as the designer increases the ADC output resolution accordingly. For example, the quantization noise of a 16-bit output resolution is $-(16 * 6.02 + 1.76) \sim -98$ dBFS. So the quantization noise has minimal impact on the SNR of a 16-bit ADC.

Clock jitter primarily affects the ADC's SNR at higher input frequencies with a full-power input signal. Sensitivity testing is often performed with a smaller (backed-off) input signal, where clock jitter noise is not a factor. Hence, the ADC noise floor is solely determined by thermal noise.

In a high-speed pipeline ADC with a switched capacitor input, thermal noise is primarily limited by the sampling circuit in the first stage (**Figure 3**). The input signal is sampled and held steady by the sampling circuit, while the flash ADC quantizes the input signal to the first N-bits. The N-bit output is then converted back to analog via the N-bit digital-to-analog converter (DAC), subtracted from the held input signal, and the residue gained up for the second pipeline stage.

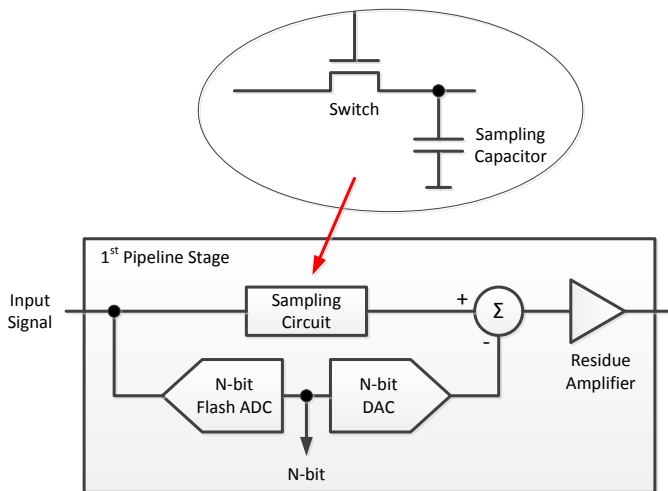


Figure 3: Sampling circuit in the pipeline ADC.

In a greatly simplified model, one can calculate the thermal noise and ADC SNR using Equations 2 and 3:

The root mean square (RMS) voltage due to the thermal noise of sampling circuit:

$$v_{THERMAL\ NOISE,RMS}^2 = \frac{k \cdot T}{C_{SAMPLING}} \quad (2)$$

ADC SNR:

$$SNR = 10 \log \frac{v_{SIGNAL,RMS}^2}{v_{THERMAL\ NOISE,RMS}^2} = \frac{v_{FULL\ SCALE,PEAK}^2}{\frac{2}{k \cdot T} \cdot C_{SAMPLING}} = 10 \log \frac{v_{FULL\ SCALE,PEAK}^2 \cdot C_{SAMPLING}}{2 \cdot k \cdot T} \quad (3)$$

This shows that, in theory, ADC thermal noise is dependent on only a few basic parameters:

- *Input full-scale swing.* The larger the input swing, the larger the SNR. Modern data converters are moving toward more advanced CMOS processes with lower power rails, which limit the full-scale swing. Furthermore, a larger swing also increases distortion in the sampling switch.
- *Sampling capacitor size.* While a larger sampling capacitor increases the SNR, it also increases the burden of the circuitry that has to drive the larger load. A larger capacitor also reduces the input bandwidth. For example, data converters that are designed to digitize signals directly at radio frequency, such as RF-sampling ADCs, inherently have a lower SNR to achieve higher-input bandwidth. A smaller sampling bandwidth translates to a longer settling time, which in turn increases the signal acquisition and impacts the maximum ADC sampling rate.
- *Temperature.* The hotter the die temperature, the worse the SNR gets. But since the temperatures are in Kelvin, a change from room temperature (290 K) to 85°C (360 K) reduces the SNR only by ~1 dB.

Other components can negatively impact ADC thermal noise as well. For example, the later pipeline stages degrade the SNR by ~1 dB. Some ADCs employ an internal front-end input buffer that adds noise similar to any buffer amplifier. The residue amplifier itself also generally adds several decibels of noise.

Summary

Modern-day radios and communications receivers need to operate in an RF environment that is more crowded than ever. Additionally, the ability to cover multiple bands simultaneously with a single receiver is driving up bandwidth requirements. In order for the receiver to maintain very good sensitivity performance in adverse and hostile blocking scenarios, high-speed data converters with a larger dynamic range and lower intrinsic noise floor are indispensable. For high-dynamic-range multiband receivers, the **ADS54J60** delivers one of the widest bandwidths of 500 MHz with one of the lowest noise floors, approaching -160 dBFS/Hz.

Additional resources

1. [ADS54J60](#) datasheet
2. Neu, Thomas. [Direct RF conversion: From vision to reality](#) (SLYY068), Texas Instruments White Paper, April 2015
3. TI [E2E™ Community High-Speed Data Converter forum](#)
4. [TI High Speed ADC Products \(>10 Msps\)](#)

About the author

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